AMENDMENTS TO THE CLAIMS:

1. (Currently amended) An output buffer apparatus comprising:

first and second power supply terminals;

an output terminal;

a main-buffer circuit including a plurality of first transistors which are ~~each~~ connected between said first power supply terminal and said output terminal and a plurality of second transistors which are ~~each~~ connected between said second power supply terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers ~~each~~ one of said first pre-drivers driving one of said first transistors in accordance with a data signal and a plurality of second pre-drivers ~~each~~ one of said second pre-drivers driving one of said second transistors in accordance with said data signal;

a plurality of first sequential circuits[[,]] which receive ~~each receiving~~ a first impedance adjusting signal in synchronization with said data signal to turn ON one of said first pre-drivers; and

a plurality of second sequential circuits[[,]] which receive ~~each receiving~~ a second impedance adjusting signal in synchronization with said data signal to turn ON one of said second pre-drivers.

2. (Currently amended) The output buffer apparatus as set forth in claim 1, wherein ~~each of~~ said first sequential circuits comprise ~~comprises~~ a first D-type flip-flop for fetching said first impedance adjusting signal in synchronization with a falling edge of said data signal, and

wherein ~~each of~~ said second sequential circuits comprise ~~comprising~~ a second D-type flip-flop for fetching said second impedance adjusting signal in synchronization with a rising edge of said data signal.

3. (Currently amended) The output buffer apparatus as set forth in claim 1, wherein ~~each of~~ said first sequential circuits comprise ~~comprises~~ a first latch circuit which is in a hold state when said data signal indicates a first value and is in a through state when said data signal indicates a second value, and

wherein ~~each of~~ said second sequential ~~latch~~ circuits comprise ~~comprising~~ a second latch circuit which is in a through state when said data signal indicates said first value and is in a hold state when said data signal indicates said second value.

4. (Currently amended) The output buffer apparatus as set forth in claim 3, wherein ~~each of~~ said first latch circuits comprise ~~comprises~~:

a first transfer gate for receiving said first impedance adjusting signal, said first transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively;

first and second inverters connected in a first feedback loop connected to said first transfer gate; and

a second transfer gate inserted into said first feedback loop, said second transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively,

wherein ~~each of~~ said second latch circuits comprise ~~comprising~~:

a third transfer gate for receiving said second impedance adjusting signal, said third transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively;

third and fourth inverters connected in a second feedback loop connected to said third transfer gate; and

a fourth transfer gate inserted into said second feedback loop, said fourth transfer gate being turned OFF and ON when said data signal indicates said first and second values,

respectively.

5. (Currently amended) An output buffer apparatus comprising:

a power supply terminal;

a ground terminal;

an output terminal;

a main-buffer circuit including a plurality of P-channel MOS transistors which are ~~each~~ connected between said power supply terminal and said output terminal and a plurality of N-channel MOS transistors which are ~~each~~ connected between said ground terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers which drive ~~each driving~~ one of said P-channel MOS transistors in accordance with a data signal and a plurality of second pre-drivers which drive ~~each driving~~ one of said N-channel MOS transistors in accordance with said data signal;

a plurality of first D-type flip-flops[[,]] which receive ~~each receiving~~ a first impedance adjusting signal in synchronization with a falling edge of said data signal to turn ON one of said first pre-drivers; and

a plurality of second D-type flip-flops[[,]] which receive ~~each receiving~~ a second impedance adjusting signal in synchronization with a rising edge of said data signal to turn ON one of said second pre-drivers.

6. (Currently amended) An output buffer apparatus comprising:

a power supply terminal;

a ground terminal;

an output terminal;

a main-buffer circuit including a plurality of P-channel MOS transistors which are ~~each~~

connected between said power supply terminal and said output terminal and a plurality of N-channel MOS transistors which are ~~each~~ connected between said ground terminal and said output terminal;

a pre-buffer circuit including a plurality of first pre-drivers which drive ~~each driving~~ one of said P-channel MOS transistors in accordance with a data signal and a plurality of second pre-drivers which drive ~~each driving~~ one of said N-channel MOS transistors in accordance with said data signal;

a plurality of first latch circuits[[,]] which receive ~~each receiving~~ a first impedance adjusting signal to turn ON one of said first pre-drivers, ~~each of~~ said first latch circuits being in a hold state when said data signal indicates a first value and being in a through state when said data signal indicates a second value;

a plurality of second latch circuits[[,]] which receive ~~each receiving~~ a second impedance adjusting signal to turn ON one of said second pre-drivers, ~~each of~~ said second latch circuits being in a through state when said data signal indicates said first value and being in a hold state when said data signal indicates said second value.

7. (Currently amended) The output buffer apparatus as set forth in claim 6, wherein ~~each of~~ said first latch circuits comprise ~~comprises~~:

a first transfer gate for receiving said first impedance adjusting signal, said first transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively;

first and second inverters connected in a first feedback loop connected to said first transfer gate; and

a second transfer gate inserted into said first feedback loop, said second transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively,

wherein ~~each of~~ said second latch circuits comprise ~~comprising~~:

a third transfer gate for receiving said second impedance adjusting signal, said third transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively;

third and fourth inverters connected in a second feedback loop connected to said third transfer gate; and

a fourth transfer gate inserted into said second feedback loop, said fourth transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively.

8. (New) The output buffer apparatus as set forth in claim 1, wherein said first sequential circuits comprise a first latch circuit which is in a hold state when said data signal indicates a first value and is in a through state when said data signal indicates a second value.

9. (New) The output buffer apparatus as set forth in claim 8, wherein said first latch circuits comprise:

a first transfer gate for receiving said first impedance adjusting signal, said first transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively.

10. (New) The output buffer apparatus as set forth in claim 9, wherein said first latch circuits further comprise:

first and second inverters connected in a first feedback loop connected to said first transfer gate.

11. (New) The output buffer apparatus as set forth in claim 10, wherein said first latch

circuits further comprise:

a second transfer gate inserted into said first feedback loop, said second transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively.

12. (New) The output buffer apparatus as set forth in claim 1, wherein said second sequential circuits comprise a second latch circuit which is in a through state when said data signal indicates said first value and is in a hold state when said data signal indicates said second value.

13. (New) The output buffer apparatus as set forth in claim 12, wherein said second latch circuits comprise:

a third transfer gate for receiving said second impedance adjusting signal, said third transfer gate being turned ON and OFF when said data signal indicates said first and second values, respectively;

third and fourth inverters connected in a second feedback loop connected to said third transfer gate; and

a fourth transfer gate inserted into said second feedback loop, said fourth transfer gate being turned OFF and ON when said data signal indicates said first and second values, respectively.

14. (New) The output buffer apparatus as set forth in claim 1, wherein a first sequential circuit in said plurality of first sequential circuits transmits an output signal to an inverter of one of said first pre-drivers.

15. (New) The output buffer apparatus as set forth in claim 1, wherein a second sequential circuit in said plurality of second sequential circuits transmits an output signal to an inverter of

one of said second pre-drivers.